## REMARKS

Claims 17-40 are all the claims pending in the application.

Applicants note that a number of editorial amendments have been made to the specification and abstract for grammatical and general readability purposes. Due to the number of changes made, a substitute specification and abstract are submitted herewith. No new matter has been added. Also enclosed is a marked-up copy of the original specification and abstract showing the changes incorporated into the substitute specification and abstract.

### I. Information Disclosure Statement

The Examiner has indicated in the Office Action that the listing of references in the Search Report is not considered to be a proper Information Disclosure Statement. While it is not clear which search report the Examiner is referring to in the Office Action, Applicants note that all of the references listed in the search reports submitted in the present application have been cited in Information Disclosure Statements. As such, Applicants note that the references cited in the search reports have been made of record in the present application.

With respect to the Information Disclosure Statement filed on September 20, 2004, Applicants note that the Examiner has not considered JP 2002-521789. In this regard, Applicants note that page 3 of the IDS filed on September 20, 2004 clearly indicates that JP 2002-521789 corresponds to WO 00/07300 (which published in English). As such, Applicants respectfully submit that the JP 2002-521789 reference should have been considered by the Examiner. In view of the foregoing, Applicants kindly request that the Examiner return a copy of the Form PTO-1449 submitted with the IDS filed on September 20, 2004 indicating that the JP 2002-

521789 has been considered.

## II. Objection to the Drawings

The Examiner has objected to the drawings for the reasons set forth on page 3 of the Office Action. In particular, the Examiner asserts that the reference characters S101, S102 and S121 are not mentioned in the specification. By this amendment, Applicants have amended the specification to include a description of S101, S102 and S121. No new matter has been added. Accordingly, Applicants kindly request that the objection be reconsidered and withdrawn.

## III. Objections to the Specification

The Examiner has objected to the abstract for the reasons set forth on page 4 of the Office Action. Applicants have amended the abstract such that it does not exceed 150 words. Accordingly, Applicants kindly request that the objection be reconsidered and withdrawn.

## IV. Objection to the Claims

The Examiner has objected to claims 18, 23, 28 and 33 for the reasons set forth on page 4 of the Office Action. In particular, Applicants note that the Examiner has indicated that claims 18, 23, 28 and 33 are improper dependent claims because they do not further limit the subject matter of a previous claim. Applicants respectfully disagree.

In particular, Applicants note that MPEP 608.01(n)(III) sets forth that the "test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, fourth paragraph) or in other words that it shall not conceivably be infringed by anything which would not also infringe the basic claim."

In addition, MPEP 608.01(n)(III) also sets forth that a "dependent claim does not lack compliance with 35 U.S.C. 112, fourth paragraph, simply because there is a question as to (1) the significance of the further limitation added by the dependent claim, or (2) whether the further limitation in fact changes the scope of the dependent claim from that of the claim from which it depends. The test for a proper dependent claim under the fourth paragraph of 35 U.S.C. 112 is whether the dependent claim includes every limitation of the claim from which it depends. The test is not one of whether the claims differ in scope."

In view of the foregoing test set forth in the MPEP for determining whether a claim is a proper dependent claim, Applicants respectfully submit that claims 18, 23, 28 and 33 are proper dependent claims. Accordingly, Applicants kindly request that the objection be reconsidered and withdrawn.

## V. Claim Rejections under 35 U.S.C. § 112, first paragraph

Claims 17-40 were rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement.

In particular, the Examiner has taken the position that the "judgement step" in claims 17, 22, 27 and 32 is not described in the specification. Applicants respectfully disagree.

Regarding claim 17, Applicants note that this claim recites the feature of "a judgment step of judging whether or not a first piece of data, which is one of a plurality of pieces of data of the error correction target code line, and a second piece of data, which is one of a plurality of pieces of data of a previous error correction code line, were located between the same pieces of sub data before being deinterleaved."

With respect to the above-noted feature in claim 17, Applicants note that step S115 of Fig. 5 and the corresponding description in the specification at page 15, line 19 through page 16, line 10 clearly provides support for such a feature.

If the Examiner does not believe that the specification at page 15, line 22 through page 16, line 10 of the specification provides support for the above-noted feature, Applicants kindly request that the Examiner explain why it is believed that such disclosure does not adequately support the above-noted feature.

Regarding claim 20, the Examiner has indicated that that the feature of judging that the first piece of data and the second piece of data do not exist between the same pieces of sub data when said first piece of data is directly subsequent to a piece of sub data or a piece of sync data in a data recording order is not supported by the specification. Again, Applicants respectfully disagree and point out that the above-noted disclosure in the specification at page 15, line 19 through page 16, line 10 provides support for such a feature.

If the Examiner does not believe that the specification at page 15, line 22 through 16, line 10 of the specification provides support for the above-noted feature in claim 20, Applicants kindly request that the Examiner explain why it is believed that such disclosure does not adequately support the above-noted feature.

Regarding claims 19, 24, 29, 34 and 37-40, Applicants note that each of these claims has been amended so as to recite that the sync data is <u>located</u> between data at predetermined intervals to configure the erasure position information of said first piece of data. Regarding such a feature, Applicants note that "SY" in the specification refers to sync data (e.g., the specification at page 4, lines 2-4 indicates that in "figure 4(b), 'SY' indicates a code line in which position information

to be used for SYNC detection is recorded"), and that the description of the sync data in the specification clearly provides support for the above-noted feature recited in amended claims 19, 24, 29, 34 and 37-40.

Regarding claims 22, 25, 27, 30, 32 and 35, Applicants respectfully submit that the features recited in these claims are supported in the specification for at least similar reasons as discussed above with respect to claims 17 and 20.

In view of the foregoing, Applicants respectfully submit that claims 17-40 comply with the written description requirement of 35 U.S.C. 112, first paragraph. Accordingly, Applicants kindly request that the above-noted rejection be reconsidered and withdrawn.

## VI. Claim Rejections under 35 U.S.C. § 112, second paragraph

Claims 17-40 were rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite.

Regarding claims 17, 18, 23, 27 and 33, the Examiner has indicated that the phrase "a plurality of pieces of sub-data" is indefinite because sub-data can already be considered as pieces of a larger data, and that it is not clear whether "pieces" is used to emphasize this fact or whether the sub-data is further divided into smaller pieces. Applicants respectfully disagree, and submit that when read in light of the specification, one of ordinary skill in the art would clearly understand the meaning of the above-noted phrase.

For example, in the specification, Applicants note that reference is made to "sub-data A" and "sub-data B" as shown in Fig. 4(b). Applicants respectfully submit that one of ordinary skill in the art would clearly understand, based on this description, as well as the remaining

description in the specification, that "sub-data A" and "sub-data B", for example, are both considered to be a piece of sub-data, and that the phrase "a plurality of pieces of sub-data" thus merely refers to more than one piece of such data, and does not in any way whatsoever refer to an individual piece of sub-data being divided into smaller pieces.

In view of the foregoing, Applicants respectfully submit that when read in light of the specification, one of ordinary skill in the art would readily understand the meaning and scope of the phrase "a plurality of pieces of sub-data".

In addition, regarding claims 17, 22, 27 and 32, the Examiner has indicated that the phrase "same pieces of data" is indefinite because it is not clear if "same" refers to pieces of data having the same values. Initially, Applicants note that claims 17, 22, 27 and 32 do not recite the phrase "same pieces of data", but instead, recite the phrase "same pieces of sub-data".

With respect to the above-noted phrase, in view of the comments above which make clear that a "piece" of sub-data refers to, for example, sub-data A or sub-data B as shown in Fig. 4(b), Applicants respectfully submit that the phrase "judging whether a first piece of data… and a second piece of data… were located between the same pieces of sub-data" would clearly be understood by one of ordinary skill in the art to refer to judging whether the first piece of data and second piece of data were located between, for example, pieces of sub-data such as sub-data A and sub-data B.

Thus, Applicants submit that when read in light of the specification, that the phrase "same pieces of sub-data" referred to in the claims would clearly be understood by one of ordinary skill in the art as referring to the actual pieces of sub-data, not the "values" of such data.

Further, with respect to claims 17, 22, 27 and 32, Applicants note that the Examiner has

also indicated that the phrase "same as erasure position information" is indefinite because it is not clear what "same" refers to. While Applicants disagree with the Examiner's position, and believe that the phrase "the same as" would clearly be understood by one of ordinary skill in the art when read in light of the specification, in order to expedite prosecution, Applicants note that the phrase "to be the same as erasure position information" has been changed to --to be identical to erasure position information--, thereby clarifying that the "erasure position information" of the first piece of data is identical to the "erasure position information" of the second piece of data.

Finally, Applicants note that MPEP §2173.02 indicates that the "Examiner's focus during the examination of a claim for compliance with the requirement for definiteness of 35 U.S.C. § 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available" and that some "latitude in the manner of expression and aptness of terms should be permitted even though the claim language is not as precise as the Examiner might desire."

In view of the foregoing, Applicants respectfully submit that claims 17-40 are in compliance with 35 U.S.C. 112, second paragraph. Accordingly, Applicants kindly request that the rejection be reconsidered and withdrawn.

## VII. Claim Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 17-20, 22-25, 27-30, 32-35, and 37-40 under 35 U.S.C. § 102(e) as being anticipated by Marchant (U.S. 6,631,492).

Claim 17 recites the feature of configuring erasure position information of said first piece of data belonging to the error correction target code line to be identical to erasure position

information of said second piece of data belonging to the previous error correction code line when said judging judges that the first piece of data and the second piece of data are both located between the same pieces of sub data. Applicants respectfully submit that Marchant does not disclose or suggest at least this feature of claim 1.

Regarding Marchant, Applicants note that this reference discloses the use of scratch detection fields 44a and 44b which are recorded at each end of a block of transverse ECC code word symbols 36' (see Fig. 7). In Marchant, it is disclosed that scratch detection occurs when a positional coincidence is found between defective scratch detection symbols 48a and 48b in consecutive scratch detection fields, with the sections of data tracks connecting such defective scratch detection symbols 48a and 48b being flagged as suspect scratch locations (see col. 6, lines 40-44). As explained in Marchant, all transverse ECC code word symbols disposed on the flagged data track segments may then be processed by erasure correction (see col. 6, lines 40-44).

Thus, in Marchant, it is possible to flag the transverse code word symbols which are disposed between two defective scratch detection symbols, and to process each of these code word symbols by erasure correction.

In this regard, Applicants note that the Examiner has indicated in the Office Action that "Marchant teach cross interleaved codes such as in U.S. Pat. No. 5,581,794, and that de-interleaving for cross interleaved codes takes place after inner code decoding, that is, after ECC correction starts, hence; Marchant teaches an embodiment where scratch detection takes place before de-interleaving on read Cross-interleaved ECC encoded data" (see Office Action at page 9). With respect to this position taken by the Examiner, however, Applicants respectfully submit that if the cross interleaved codes described in U.S. Patent No. 5,581,794 were applied to

Marchant, it would <u>not</u> be possible to determine the correct position where a scratch has occurred.

Accordingly, because the use of cross-interleaved codes in Marchant would prevent the configuration of a correct erasure position, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious the above-noted feature of configuring erasure position information of said first piece of data belonging to the error correction target code line to be identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judging judges that the first piece of data and the second piece of data are both located between the same pieces of sub data, as recited in claim 17.

In view of the foregoing, Applicants respectfully submit that claim 17 is patentable over the cited prior art, an indication of which is kindly requested. Claims 18-20 and 37 depend from claim 17 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 22, Applicants note that this claim recites the feature of configuring erasure position information of said first piece of data belonging to the error correction target code line to be identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judging judges that the first piece of data and the second piece of data are both located between the same pieces of sub data.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 22 is patentable over the cited prior art, an indication of which is kindly requested. Claims 23-25 and 38 depend from claim 22 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 27, Applicants note that this claim recites the feature of a configuration means for configuring erasure position information of said first piece of data belonging to the error correction target code line to be identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judgement means judges that the first piece of data and the second data piece of data are both located between the same pieces of sub data.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 27 is patentable over the cited prior art, an indication of which is kindly requested. Claims 28-30 and 39 depend from claim 27 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 32, Applicants note that this claim recites the feature of a configuration means for configuring erasure position information of said first piece of data belonging to the error correction target code line to be identical to erasure position information of said second piece of data belonging to the previous error correction code line when said judgment means judges that the first piece of data and the second piece of data are both located between the same pieces of sub data.

For at least similar reasons as discussed above with respect to claim 17, Applicants respectfully submit that Marchant does not disclose, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 32 is patentable over the cited prior art, an indication of which is kindly requested. Claims 33-35 and 40 depend from claim 32 and are therefore considered patentable at least by virtue of their dependency.

## VIII. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 21, 26, 31 and 36 under 35 U.S.C. § 103(a) as being unpatentable over Marchant (U.S. 6,631,492) in view of Eachus (U.S. 3,685,016).

Claim 21 depends from claim 17; claim 26 depends from claim 22; claim 31 depends from claim 27; and claim 36 depends from claim 32. Applicants respectfully submit that Eachus does not cure the above-noted deficiency of Marchant, with respect to claims 17, 22, 27 and 32. Accordingly, Applicants respectfully submit that claims 21, 26, 31 and 36 are patentable at least by virtue of their dependency.

## IX. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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SPECIFICATION

# INTERLEAVED DATA ERROR CORRECTION METHOD AND DEVICE

## TECHNICAL FIELD

The present invention relates to an error correction method and an error correction apparatus and, more particularly, to an error correction method and an error correction apparatus~~circuit~~ for interleaved data.

## BACKGROUND ART

Conventionally, in a system performing recording/playback of digital data, since errors might occur in data during playback or recording, it is necessary to detect and correct the errors. Reed-Solomon codes are well known as error correcting codes to be used for such error correction.

Hereinafter, a conventional error correction method will be described with reference to figure 1, taking as an example a case where data recorded on a DVD as an optical medium are subjected to error correction using Reed-Solomon codes. Figure 1 is a diagram indicating that data recorded on a DVD are divided into error correction unit blocks (ECC blocks).

Initially, Reed-Solomon-coded data are subjected to Reed-Solomon decoding, and error correction is carried out in a direction C1 or a direction C2 shown in figure 1. At this time, a position polynomial and a numeric value polynomial are

generated from the Reed-Solomon-decoded data, and the roots thereof are obtained to obtain an error position and an error numeric value. When there exists an error exceeding the error correctability in each code line, the code line is regarded as an uncorrectable code line, and information relating to this uncorrectable code line is stored as erasure position information. When error correction for all code lines in one ECC block is completed with respect to one of the direction C1 and the direction C2, error correction is carried out in the other direction using the erasure position information. In this way, when the position of error data has previously been known, since the erasure position information indicating the position of error data can be utilized, only a numeric value polynomial should be generated when generating the above-mentioned polynomials. As a result, the error correctability can be enhanced. The above-mentioned conventional method utilizes that, in a DVD, the order in which the data are recorded and the order in which the code lines are arranged are in the same direction C1, and thereby all ~~of~~ settings of erasure position information are the same in one ECC block.

For example, it is assumed that initially error correction is carried out in the direction C1, and the 50th, 90th, 130th, and 200th code lines are uncorrectable code lines. In this case, as shown in figure 3, when performing error correction in the direction C2 that is the next error correction direction, the

50th, 90th, 130th, and 200th bytes are designated as erasure positions on the basis of the erasure position information indicating the previous uncorrectable code lines, thereby enhancing the error correctability in the direction C2.

However, if the recording order and coding order of the recorded data are the same like data recorded on a DVD, the error correctability to correct continuous data errors (burst errors) that occur due to contamination on the disc surface is degraded as the density of the recorded data is increased. Accordingly, in order to avoid such degradation in the error correctability due to large-scale burst errors that occur in the data, there has been proposed an error correction method in which data to be subjected to error correction is subjected to interleaving (P2002-521789A).

In this error correction method, under the state where the recording order and coding order for data in an ECC block are intersected, data to be subjected to error correction is divided into main data (MD) as recorded information and sub data (SD) to be used for calculating erasure position information of the main data, and the main data is subjected to interleaving. Figures 4(a) to 4(c) show an ECC block in a rewritable area of a high-density optical disc in which interleaved data are stored. As shown in figure 4(a), since a 32-byte parity data area is added to the ECC block, it is possible to set erasure position information up to 32 positions for every code line when

performing error correction on the main data. In figure 4(b), "SY" indicates a code line in which position information to be used for SYNC detection is recorded. Further, the sizes of the main data and parity data shown in figures 4(a) to 4(c) are merely examples, and are not restricted thereto.

Hereinafter, an error correction processing for the ECC block shown in figure 4 will be described.

Initially, the sub data is subjected to error correction, and erasure position information of the main data is calculated on the basis of the result of the error correction. Then, the erasure position information is used when performing error correction on the main data. Thereby, the error correctability for the main data can be enhanced. The main data in the areas between the sub data or the areas between the SY and the sub data have the same erasure position information. For example, when errors exist in sub data A and sub data B shown in figure 4(b) and error correction is carried out, it is assumed that a burst error occurs in a main data area $\alpha$ sandwiched between the sub data A and B. When performing error correction on the main data, erasure position information calculated from the sub data A and B is set as erasure position information of the main data in the area $\alpha$. In the ECC block shown in figure 4, since the main data is interleaved in the row direction (data recording order), setting of the erasure position information in the column direction (coding order) is different from that in the ECC block

shown in figure 1, that is, the erasure positions are not the same in one ECC block. Accordingly, it is necessary to set erasure position information for every code line. For this purpose, 9,728 ($32 \times 304$) times of erasure position information settings are required for once correcting the main data in the ECC block.

There has also been proposed an error correction apparatus for realizing the above-mentioned error correction method of performing error correction using previously known erasure position information. As examples of error correction apparatuses of this type, there have been proposed an apparatus in which a central processing unit (CPU) sets erasure position information on an error correction circuit (first error correction apparatus), and an apparatus in which an error correction circuit itself accesses a memory circuit in which erasure position information is stored, and obtains the erasure position information (second error correction apparatus).

However, the above-mentioned error correction apparatuses have the following drawbacks. First of all, in the first error correction apparatus, when performing error correction on interleaved data as shown in figure 4, 9,728 times of erasure position settings are required from the CPU to the error correction circuit. Therefore, the time required for error correction relative to the time required for the whole processing by the CPU is increased. As a result, when the error correction

apparatus is constituted as an integrated circuit, the performance of the whole integrated circuit is significantly degraded.

On the other hand, in the second error correction apparatus, since the error correction circuit itself accesses the memory circuit in which the erasure position information has already been stored, to obtain the erasure position information, when performing error correction on interleaved data as shown in figure 4, 248 accesses per code line are made to obtain the erasure position information. That is, 75,392 times of accesses are made to perform error correction on all main data, and much time is spent for error correction.

As described above, the first and second error correction apparatuses take much time for error correction.

Therefore, the present invention has an object to achieve a reduction in time required for error correction in a method for performing error correction on interleaved data. Further, it is another object of the present invention to achieve a reduction in time required for error correction in an apparatus for performing error correction on interleaved data.

## SUMMARY~~DISCLOSURE~~ OF THE INVENTION

According to a first aspect~~Claim 1~~ of the present invention, an error correction method for performing error correction on data which are interleaved and are composed of plural code lines,

comprises: a step of giving parameters for tracking down errors in the respective code lines; a rearrangement step of rearranging the code lines in the order in which error correction is to be carried out; a judgement step of, with a code line to be subjected to error correction being a target code line, comparing the parameter of the target code line that is given in the step of giving the parameters, with the parameter which is used when performing error correction on a code line that is previous to the target code line in the error correction order, and judging, according to the result of the comparison, as to which parameter is to be used for tracking down an error in the target block, the parameter in the target code line or the parameter which is used when performing error correction on the code line that is previous to the target code line in the error correction order; and an error correction step of performing error correction on the data for every code line, using the parameter.

According to the present invention, in the error correction method for performing error correction on the interleaved data using the parameters for tracking down errors, the time required for the data error correction can be reduced.

According to a second aspect~~Claim 2~~ of the present invention, in the error correction method described in the first aspect~~Claim 1~~, the parameter for tracking down an error in the target code line is determined before performing error correction on the target code line.

According to a third aspect~~Claim 3~~ of the present invention, in the error correction method described in the first aspect~~Claim 1~~, in the rearrangement step, the order of the code lines of the data are rearranged at intervals of at least two lines.

According to a fourth aspect~~Claim 4~~ of the present invention, the error correction method described in the first aspect~~Claim 1~~ further includes a first error correction incapability judgement step of judging whether or not the target code line is incapable of being subjected to error correction, on the basis of the parameter; wherein error correction is carried out without using the parameter when the result of the judgement in the first error correction incapability judgement step indicates "incapable of error correction".

According to a fifth aspect~~Claim 5~~ of the present invention, the error correction method defined in the fourth aspect~~Claim 4~~ further includes a second error correction incapability judgement step of judging whether or not a code line that is previous to the target code line in the error correction order was incapable of being subjected to error correction; wherein the target code line is subjected to error correction using the parameter of the target code line when the result of the judgement in the second error correction incapability judgement step indicates "incapable of error correction".

According to a sixth aspect~~Claim 6~~ of the present invention, in the error correction method defined in the first aspect~~Claim 1~~,

the data are stored in an optical medium.

According to a seventh aspect~~Claim 7~~ of the present invention, an error correction apparatus for performing error correction on data which are interleaved and are composed of plural code lines, comprises: a first memory circuit for storing data to be subjected to error correction; a first control circuit for performing control so as to rearrange data being transferred from the first memory circuit to the error correction circuit, in the order in which the data are to be subjected to error correction; an error correction circuit for performing error correction on the data stored in the first memory circuit, for each code line, using parameters for tracking down errors in the code lines; a storage unit for storing parameters that have been used for error correction by the error correction circuit; a comparator for comparing the parameter of the target code line with the parameter which has been used when performing error correction on a code line that is previous to the target code line in the error correction order and is stored in the storage unit; wherein the control circuit rearranges the order of the code lines to be subjected to error correction, at intervals of at least two lines, and the error correction circuit performs error correction on the target code line, according to the result of the comparison by the comparator, using, as the parameter for tracking down an error in the target code line, the parameter of the target code line or the parameter which has been used when

performing error correction on a code line that is previous to the target code line in the error correction order.

According to the present invention, in the error correction apparatus for performing error correction on the interleaved data using the parameters for tracking down errors, the time required for the data error correction can be reduced.

According to an eighth aspect~~Claim 8~~ of the present invention, an error correction apparatus defined in the seventh aspect~~Claim 7~~ further includes a second memory circuit for storing the parameters, and a second control circuit for performing control so as to read the parameters from the second memory circuit, and transferring the parameters.

According to a ninth aspect~~Claim 9~~ of the present invention, in the error correction apparatus defined in the seventh aspect~~Claim 7~~, the storage unit is provided with a group of registers.

According to a tenth aspect~~Claim 10~~ of the present invention, in the error correction apparatus defined in the ninth aspect~~Claim 9~~, the group of registers hold the parameters which are obtained from the second memory circuit through the second control circuit.

According to an eleventh aspect~~Claim 11~~ of the present invention, in the error correction apparatus defined in the tenth aspect~~Claim 10~~, the group of registers includes a first register for holding the number of parameters obtained from the second

memory circuit; and a second register for holding the parameters obtained from the second memory circuit.

According to a twelfth aspect~~Claim 12~~ of the present invention, in the error correction apparatus defined in the eleventh aspect~~Claim 11~~, the second register is a shift register.

According to a thirteenth aspect~~Claim 13~~ of the present invention, in the error correction apparatus defined in the eighth aspect~~Claim 8~~, the second control circuit generates addresses to be used when reading the parameters from the second memory circuit on the basis of the information stored in the group of registers.

According to a fourteenth aspect~~Claim 14~~ of the present invention, in the error correction apparatus defined in the eighth aspect~~Claim 8~~, the data comparator compares the parameters stored in the second memory circuit with the parameters stored in the second register.

According to a fifteenth aspect~~Claim 15~~ of the present invention, in the error correction apparatus defined in the seventh aspect~~Claim 7~~, the first control circuit performs control such that at least two code lines of data to be subjected to error correction are simultaneously transferred from the first memory circuit to the error correction circuit; and the error correction circuit has a means capable of receiving at least two code lines of data simultaneously.

According to a sixteenth aspect~~Claim 16~~ of the present

invention, in the error correction apparatus defined in the seventh aspect~~Claim 7~~, the data are stored in an optical medium.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram illustrating an example of construction of an ECC block on a DVD.

Figure 2 is a diagram illustrating an example of error correction with respect to C1 direction in the ECC block shown in figure 1.

Figure 3 is a diagram illustrating an example of error correction in C2 direction in the ECC block shown in figure 1.

Figures 4(a)-4(c) are diagrams illustrating an example of construction of an ECC block in a rewritable area on a high-density optical disc in which interleaved data are stored.

Figure 5 is a flowchart illustrating the procedure of error correction performed on main data in the ECC block shown in figure 4.

Figure 6 is a schematic diagram illustrating an example of construction of an error correction apparatus according to a first embodiment of the present invention.

Figure 7 is a schematic diagram illustrating the order in which main data are transferred in the error correction apparatus shown in figure 6.

Figure 8 is a schematic diagram illustrating the order in which main data are subjected to error correction in the error

correction apparatus shown in figure 6.

## DETAILED DESCRIPTION OF ~~BEST MODE TO EXECUTE~~ THE INVENTION

(Embodiment 1)

A first embodiment of the present invention will be described with reference to figures 5 to 8. An error correction method according to the first embodiment is a method for performing error correction on interleaved data in an ECC block, as shown in figure 4. Therefore, initially error correction is performed on sub data, and erasure position information of main data is calculated on the basis of the result of error correction, and the information is used when performing error correction on the main data, as described for the conventional example. That is, the erasure position information is a parameter for tracking down an error in each code line of the main data. When the data in the ECC block has been subjected to Reed-Solomon coding, error position information is obtained from a position polynomial that is calculated at Reed-Solomon decoding, and the error position information is calculated by using a specific algorithm to obtain erasure position information.

Hereinafter, the procedure of main data error correction will be described in detail using a flowchart shown in figure 5. Initially, step S101 represents start of the processing. In step S102, 0 is set to the code line n. Then, erasure position information about all byte positions in a code line 0 is set, and

the number of erased data S in the code line 0 is counted (step S104). Before performing step S104, an error correction incapability flag indicating whether the code line is incapable of being subjected to error correction or not is initialized (step S103). When the number of erased data S counted in step S104 is equal to or smaller than 32, error correction is carried out using the erasure position information (step S106). On the other hand, when the number of erased data S is equal to or larger than 33, the error correction incapability flag is incremented from 0 to 1 (step S107), and error correction is carried out without using the erasure position information (step S108). The reason is as follows. As shown in figure 4, since, in the ECC block, the parity data area has 32 bytes, error correction can be carried out using the erasure position information when the number of erased data S is equal to or smaller than 32, but error correction cannot be carried out using the erasure position information when the number of erased data S is equal to or larger than 33. Next, the number of code lines on which error correction has been completed is incremented by 2 (step S109). That is, since interleaving has been done so that every other code line should be subjected to error correction, the code lines are rearranged in the error correction order. That is, after performing error correction on the code line 0, even-numbered code lines (code lines 2, 4, 6, 8, ..., 302) are subjected to error correction, and thereafter, odd-numbered code

lines (code lines 1, 3, 7, 9, ..., 303) are subjected to error correction. When the code lines are rearranged in the error correction order, the code line 1 becomes the 153rd code line counting from the first code line. Since, in this embodiment, error correction is performed on the ECC block shown in figure 4, the number of code lines is incremented by 2 in step S109. However, the number of code lines to be incremented depends on how many code lines have been skipped when the code lines to be subjected to error correction are arranged in the error correction order. For example, when every third code line is~~lines are~~ to be subjected to error correction, the number of code lines is incremented by 3 in step S109. After step S109, if the number of code lines incremented is 305 (n = 305), it is judged that setting of erasure position information is done for all of the code lines (step S110 and step S121). On the other hand, when the number of code lines incremented is not 305, it is judged whether setting of erasure position information for the even-numbered code lines has been completed or not (step S111). When the result of the judgement in step S111 is "yes", setting of erasure position information for all byte positions in the code line 1 is started. On the other hand, when the result of the judgement in step S111 is "No", it is judged as to whether the previously error-corrected code line was incapable of being subjected to error correction or not (step S113). In this first embodiment, when the immediately previous code line (i.e., the

code line 0 when the result of increment in step S109 is n = 2) is judged as to whether it is an error-incorrectable code line or not. When the result of the judgement in step S113 is "Yes", steps S103 to S108 are repeated to set erasure position information for the target code line and, further, the number of erased data is counted. On the other hand, when the result of the judgement in step S113 is "No", all of the byte positions in the target code line are subjected to judgement as to whether the byte positions are boundaries with the sub data area or the SY area (step S115), starting from the byte position i = 0 (step S114). The reason is as follows. Since the main data between sub data or the main data between sub data and SY have the same erasure position information, erasure position information should be set at only the boundary between the main data area and the sub data area or the SY area. To be specific, when the code lines are rearranged in the error correction order, the byte positions of the code line 0, code line 38, code line 76, code line 114, code line 152, code line 190, code line 228, and code line 266 are boundaries with the sub data area or the SY area. When the result of the judgement in step S115 is "No", since the erasure position information at the same byte position in the previous code line is used, the processing goes to step S119 to judge whether the next byte position is a boundary with the sub data area or the SY area. On the other hand, when the result of the judgement in step S115 is "Yes", i.e., when the byte position

is a boundary with the sub data area, it is judged whether the erasure position information in the target byte position in the target code line indicates "erasure" or not (step S116). When the result of the judgement in step S116 indicates "erasure", the number of erased data is incremented (step S117). When it does not indicate "erasure", the number of erased data is decremented (step S118). The operations of the above-mentioned steps S115 to S118 are repeated up to the final byte in one code line (i = 248) (step S119). When erasure information setting is completed up to the final byte in the one code line (step S120), the processing goes to step S105 to execute error correction.

As described above, in the error correction method according to the first embodiment, as for the code line 0 and the code line 1 in the ECC block, the corresponding erasure position information is set for all of the byte positions. Then, the code lines are rearranged in the error correction order, and it is judged whether the corresponding erasure position information indicates "erasure of data" or not, for all of the byte positions at the boundary between the main data area and the sub data area or the SY area in the code line. Then, erasure position information is set for only positions where erasure position information should be newly obtained. As for the other byte positions, erasure position information of the previous code line at the same byte position in the error correction order is set. However, when the previous code line is an error-incorrectable

code line, erasure position information is set for all of the byte positions in the next code line that is next to the error incorrectable code line in the error correction order. As for the subsequent code lines, erasure position information thereof is set again until the target byte position reaches the boundary position between the main data area and the sub data area or the SY area. Thereby, the number of settings of erasure position information is reduced as compared with the case where erasure position information should be set for all positions in all code lines, resulting in a reduction in the time required for error correction.

Hereinafter, an error correction apparatus that realizes the above-mentioned error correction method will be described with reference to figures 6 to 8. Figure 6 is a block diagram illustrating an example of construction of an error correction apparatus. As shown in figure 6, the error correction apparatus comprises a first memory circuit 61, a second memory circuit 62, a first control circuit 63, a second control circuit 64, an error correction circuit 65, a data comparator 66, a register unit 67, and a third control circuit 68. The register unit 67 comprises a first register 67a, a second register 67b, a third register 67c, and a fourth register 67d. The first memory circuit 61 stores data to be subjected to error correction. The first control circuit 63 controls data transfer from the first memory circuit 61 to the error correction circuit 65. The error correction

circuit 65 performs error correction for data transferred from the first control circuit 63. The error correction circuit 65 is provided with a reception means (not shown) for receiving two or more code lines of data. For example, it is provided with, as the reception means, a holding circuit for holding two or more code lines of data. The second memory circuit 62 stores information relating to error correction. In this first embodiment, it stores erasure position information. The second control circuit 64 controls transfer of information from the second memory circuit 62 to the register unit 67. The first register 67a holds the number of information (parameter values) obtained from the second memory circuit 64. Since the parameter values indicate the erasure position information, the number of parameter values is the number of erasure position information. The second register 67b is a shift register, and holds the erasure position information obtained from the second memory circuit 62, as parameter values. The data comparator 66 compares the parameter values stored in the second register 67b with the parameter values transferred from the second memory circuit 62. Since a shift register is used as the second register 67b, it is not necessary to provide a data comparator 66 for every parameter value, and comparison can be carried out for every parameter value shifted, resulting in a reduction in the circuit scale of the error correction apparatus. The third register 67c holds the number of code lines counted by the third control circuit 68.

The fourth register 67d holds the number of bytes counted by the third control circuit 68.

Further, the respective circuits mentioned above are connected to each other via an internal bus. The internal bus comprises an address bus, a data bus, and control buses such as a read strobe, write strobe, and a reset signal.

Hereinafter, a description will be given of the operation of the error correction apparatus constructed as described above, when performing error correction for the ECC block shown in figure 4.

First of all, the data stored in the first memory circuit 61 is transferred to the error correction circuit 65 under control of the first control circuit 63. Figure 7 shows an example of setting of the order in which data are transferred to the error correction circuit 65. As shown in figure 7, the data transfer order is set not for every code line (0th code line, 1st code line, 2nd code line, ..., 303rd code line) but for every other code line (0th code line, 2nd code line, 4th code line, 302nd code line, 1st code line, 3rd code line, ..., 303rd code line). This is because, in the ECC block shown in figure 4, the data have been interleaved so that every two code lines are skipped with respect to the coding order. That is, the first control circuit 63 rearranges the code lines at intervals of two or more lines.

The error correction circuit 65 performs error correction in

the order in which the data are to be transferred through the first control circuit 63. Hereinafter, the error correction processing will be described with reference to figure 8. Figure 8 shows an image of the order in which the main data are subjected to error correction. Initially, error correction is performed on the sub data, and then erasure position information of the main data is calculated on the basis of the result of the error correction. The erasure position information is stored in the second memory circuit 62. After the error correction for the sub data, initially the code line 0 of the main data is transferred from the first memory circuit 61 through the first control circuit 63 to the error correction circuit 65. On receipt of the code line 0, the error correction circuit 65 obtains all of 248 bytes of erasure position information corresponding to the code line 0 from the second memory circuit 62 through the second control circuit 64. Then, the error correction circuit 65 performs error correction starting from the code line 0. At this time, the third control circuit 68 counts the number of erased data on the basis of the erasure position information. The result of the count is stored in the first register 67a. When the number of erased data does not exceed 32, error correction is carried out using the erasure position information. The erasure position information used by the error correction circuit 65 is stored in the register 67b. On the other hand, when the number of erased data exceeds 32, it is

judged that error correction is impossible, and error correction is carried out without using the erasure position information. The erasure position information that is set at error correction is held by the second register 67b.

Next, in contrast to the order in which the code lines are actually stored in the recording disc, the first control circuit 63 transfers the code line 2 to the error correction circuit 65, i.e., one code line is skipped. The error correction circuit 65 performs error correction on the code line 2 by reusing the erasure position information that is stored in the second register 67b at error correction for the code line 0. This is because, as shown in figure 4(b), the 0th to 37th code lines have the same erasure position information. However, when the target code line is at the boundary between the main data area and the sub data area or the SY area, the already-obtained erasure position information cannot be reused, and therefore, erasure position information corresponding to the target code line is newly obtained from the second memory circuit 62 through the second control circuit 64 to perform error correction. By the way, addresses required for reading the erasure position information are generated by the second control circuit 64 on the basis of the information stored in the register unit 67. In the ECC block shown in figure 4, when the code lines are rearranged in the error correction order, the 38th code line, the 76th code line, the 114th code line, the 152nd code line, the 190th code

line, the 228th code line, and the 266th code line are code lines at the boundary. The third control circuit 68 judges whether the target code line is a code line at the boundary or not. Further, when the number erased data positions in the code line previous to the target code line exceeds 32, erasure position information is newly obtained for the next code line (target code line) in the error correction order, from the second memory circuit 62 through the second control circuit 64.

The data comparator 66 compares the parameter values stored in the second memory circuit 62 with the parameter values held by the second register 67b, with respect to all of the byte positions in the code line to be read from the second memory circuit 64, i.e., the positions where the erasure position information shown in figure 8 must be obtained. The number of bytes compared is counted by the third control circuit 68, and the result of the count is held by the fourth register 67d. Further, the number of erased data obtained from the erasure position information is also counted by the third control circuit 68, and the result of the count is held by the first register 67a. On the basis of the result of the comparison, the third control circuit 68 judges that it is not necessary to read the erasure position information which is already held by the second register 67b, from the second memory circuit 62, and the error correction circuit 65 performs error correction using the erasure position information held by the second register 67b.

As described above, the error correction apparatus according to the first embodiment reads all of erasure position information corresponding to the code lines 0 and 1 in the ECC block, from the second memory circuit 62. Then, the code lines are rearranged in the error correction order, and thereafter, the erasure position information stored in the second memory circuit 62 is compared with the erasure position information stored in the second register 67b, with respect to all of the byte positions in the code line at the boundary between the main data area and the sub data area or the SY area, and the second memory circuit 62 is accessed to obtain erasure position information for only byte positions where erasure position information should be newly obtained. However, when the code line previous to the target code line is an error-incorrectable code line, erasure position information corresponding to the next code line (target code line) in the error correction order is read from the memory circuit 62. Thereby, the number of settings of erasure position information is reduced as compared with the case where erasure position information is set for all positions in all code lines, resulting in a reduction in time required for error correction.

While the error correction apparatus shown in figure 6 includes two memory circuits, three control circuits, and two registers, the numbers of these circuits are not restricted thereto. For example, the error correction apparatus may be provided with one or more than two memory circuits, control

circuits, and registers.

While in this first embodiment the second register 67 shown in figure 6 is a shift register, the present invention is not restricted thereto.

## APPLICABILITY IN INDUSTRY

The present invention is suitable for a high-density optical disc recording/reproduction apparatus that records or reproduces interleaved data.

ABSTRACT

In an error correction method for performing error correction on an error correction unit block in which main data are interleaved, after rearranging code lines in the order of error correction, it is judged whether the corresponding erasure position information indicates "erasure of data" or not with respect to only byte positions in a code line at a boundary between a main data area and a sub data area or a SY area, and erasure position information is set for only positions where erasure position information should be newly obtained. With respect to other byte positions, erasure position information at the same byte positions in a previous code line in the error correction order is set. ~~However, when the previous code line is an error-incorrectable code line, erasure position information is set for all byte positions in a code line that is next to the incorrectable code line in the error correction order. With respect to the subsequent code lines, erasure position information is set until the target byte position reaches the next boundary between the main data area and the sub data area or the SY area. Thereby, the time required for error correction can be reduced.~~